

FIG. 1

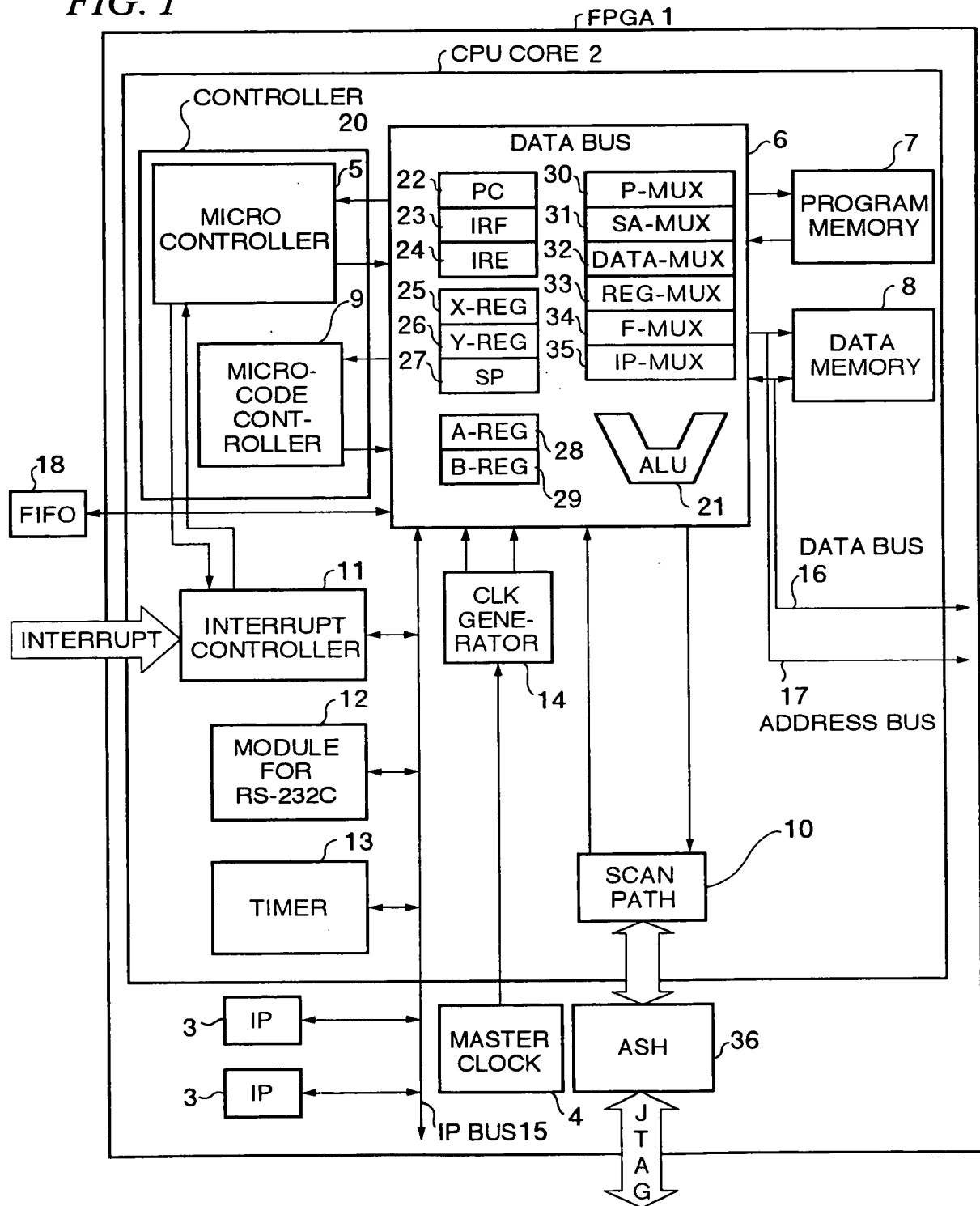


FIG. 1

FIG.2

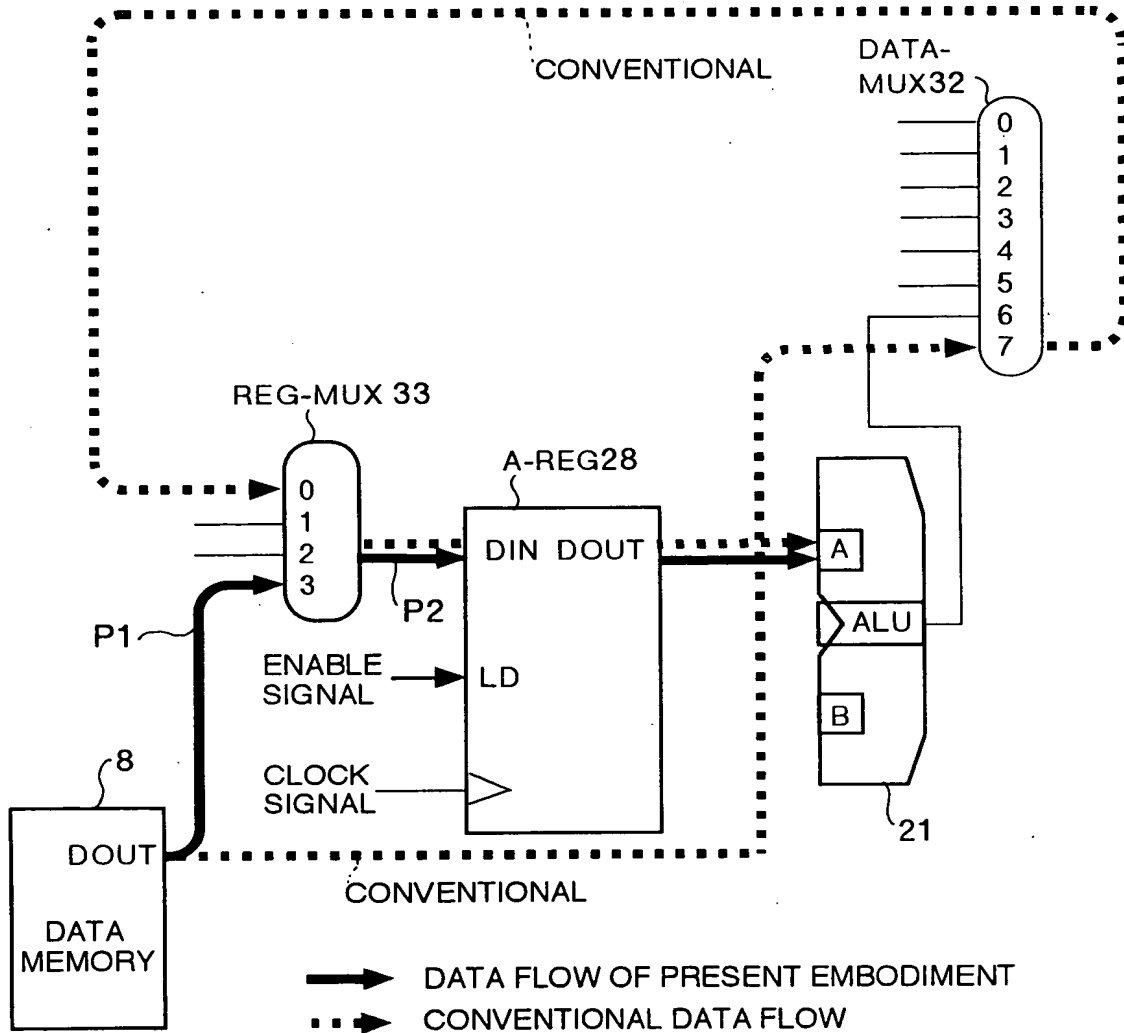
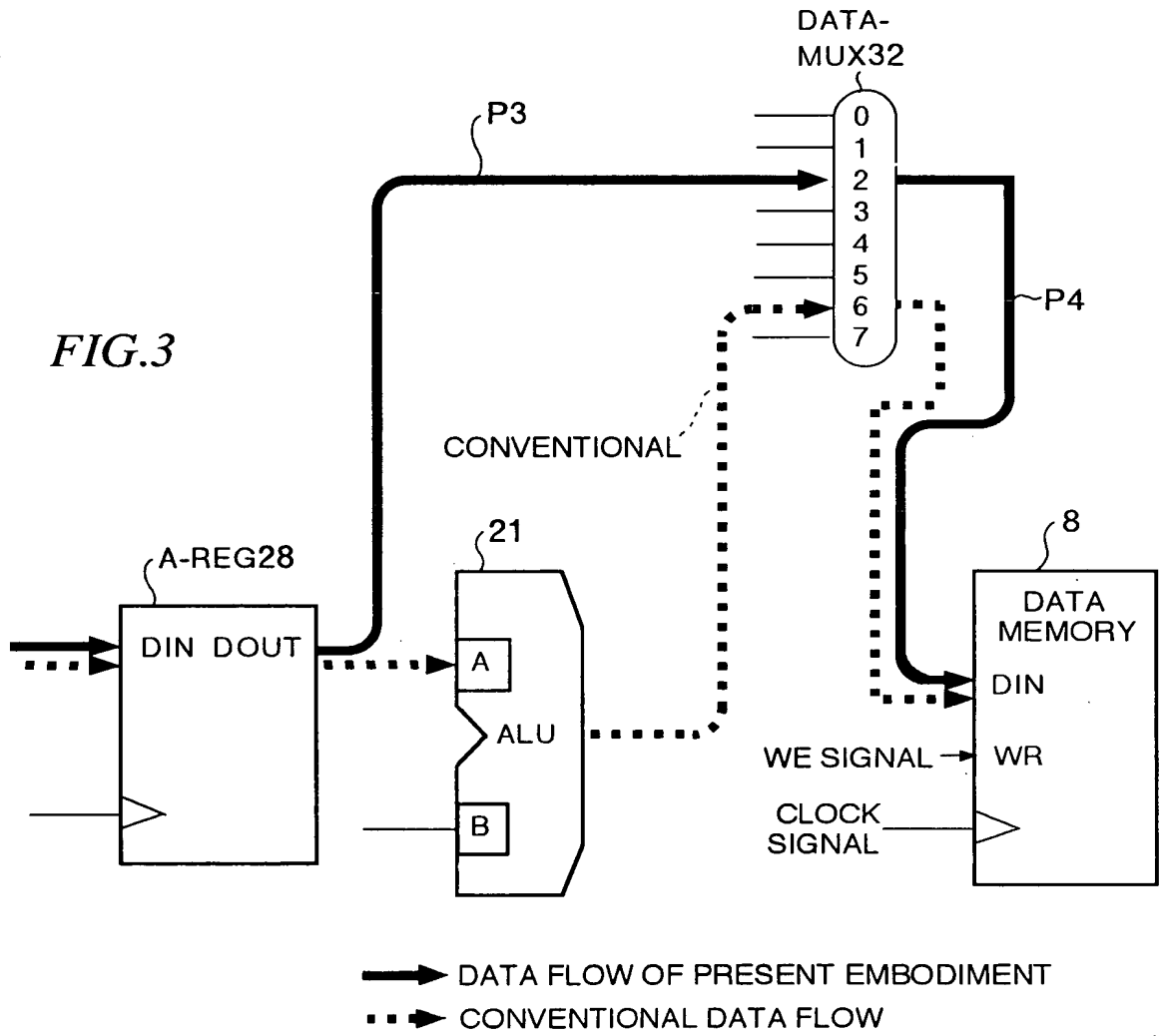


FIG.3



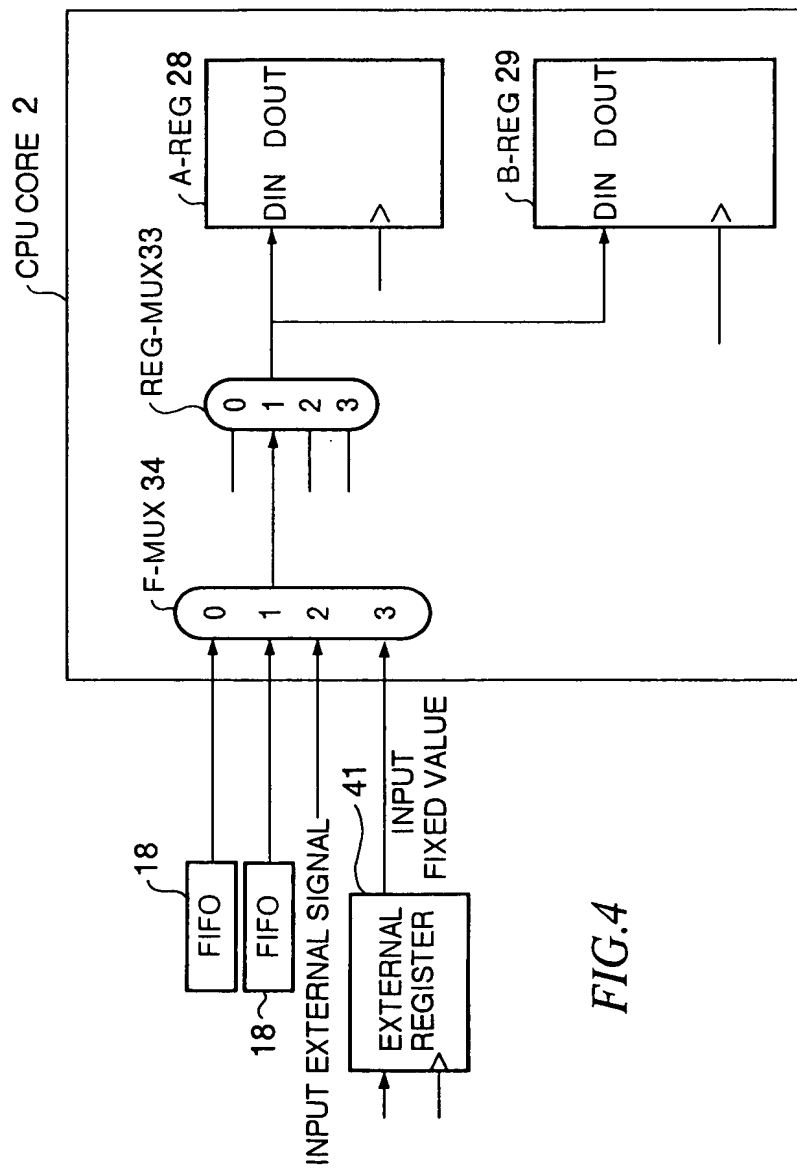


FIG. 4

FIG.5

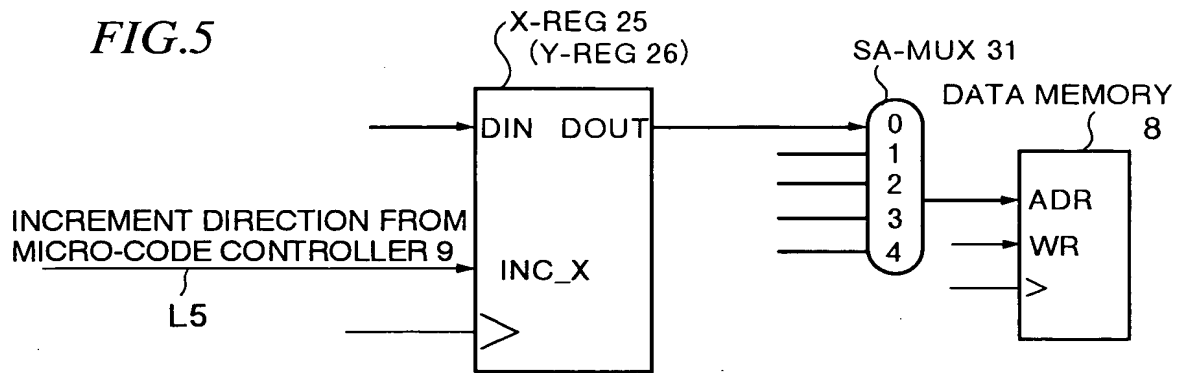


FIG.6 PRIOR ART

EXAMPLE OF CONTROL IN SINGLE CLOCK (IN LDA & STA CONTINUOUS COMMAND)

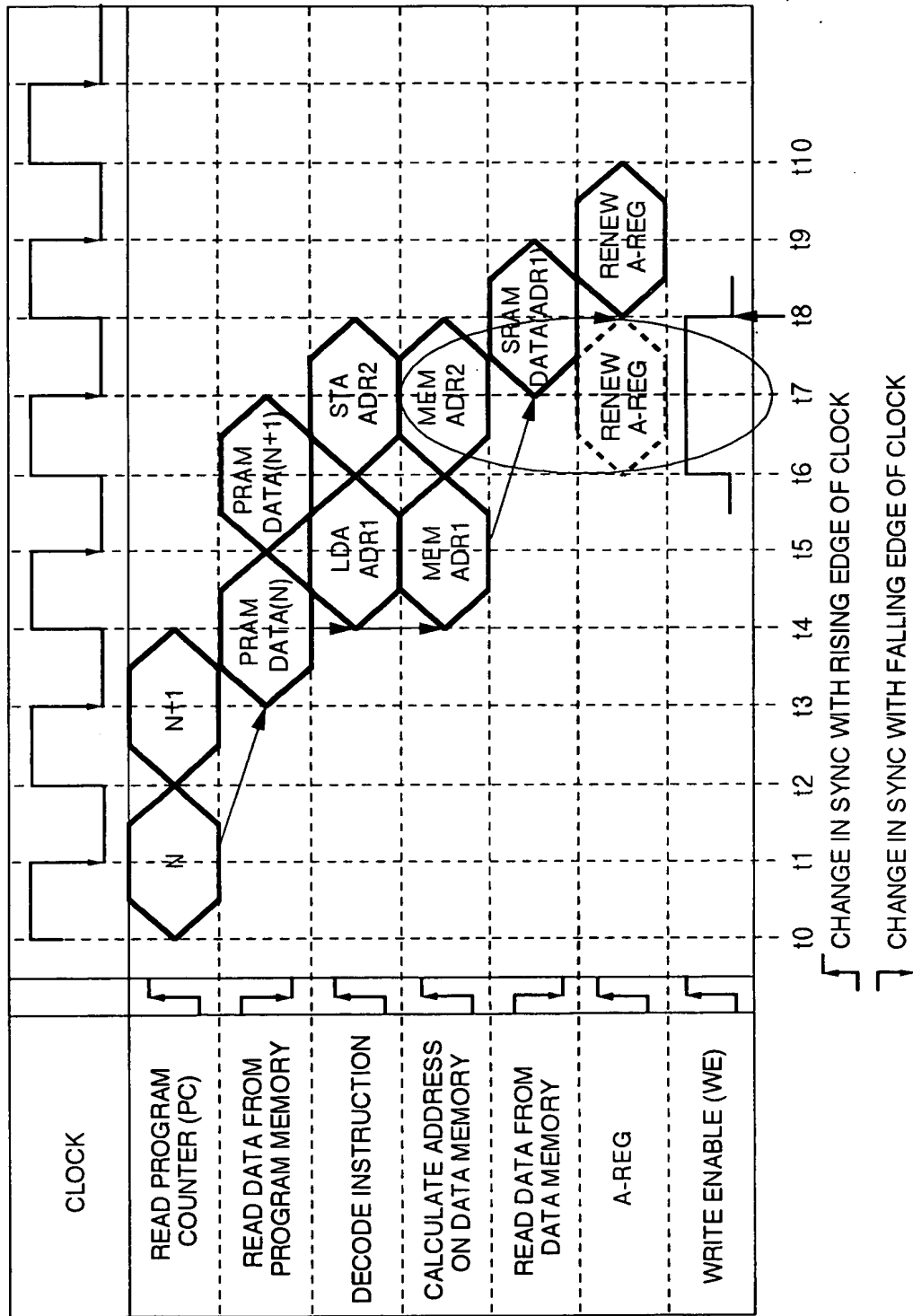
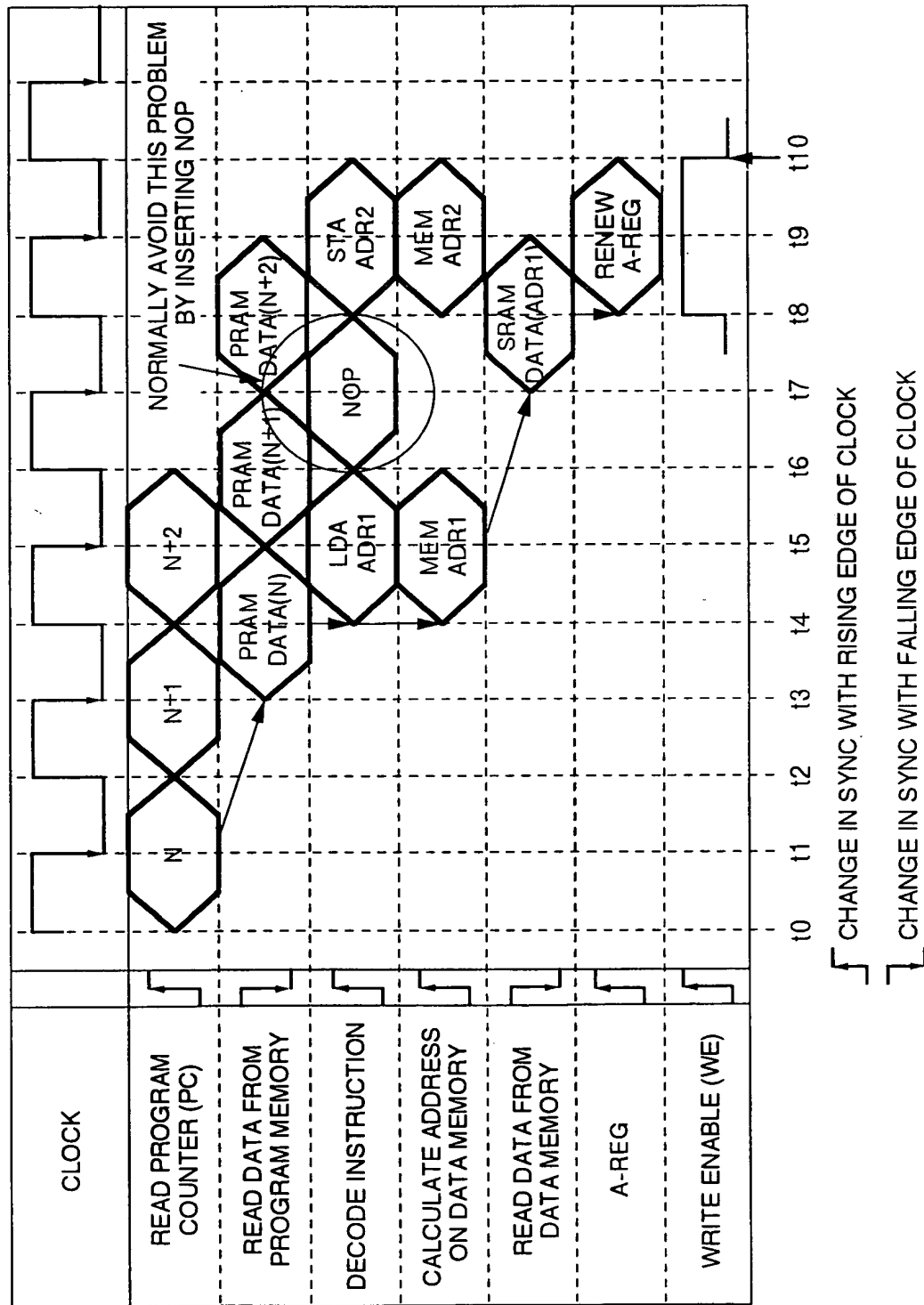


FIG. 7

EXAMPLE OF SOLUTION BY INSERTING NOP



CONTROL METHOD OF CPU CORE IN PRESENT EMBODIMENT

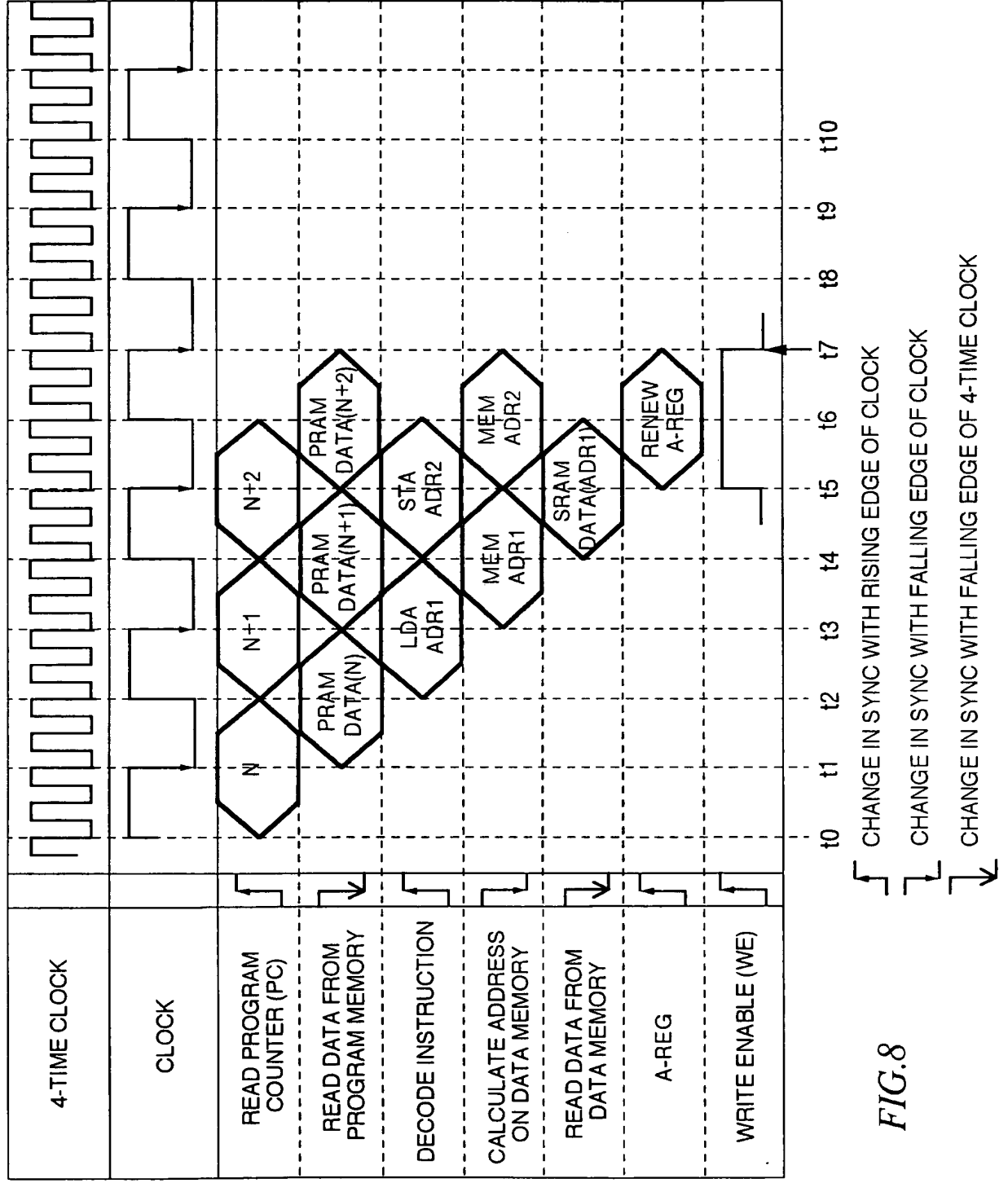
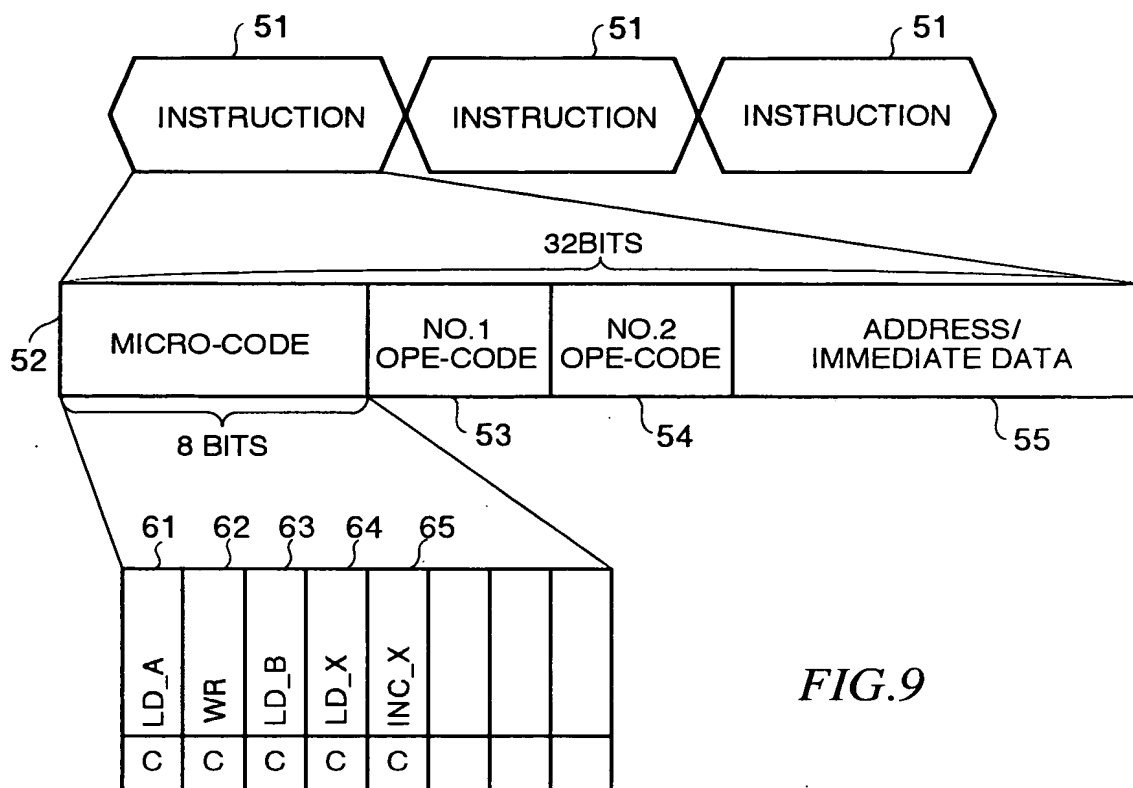
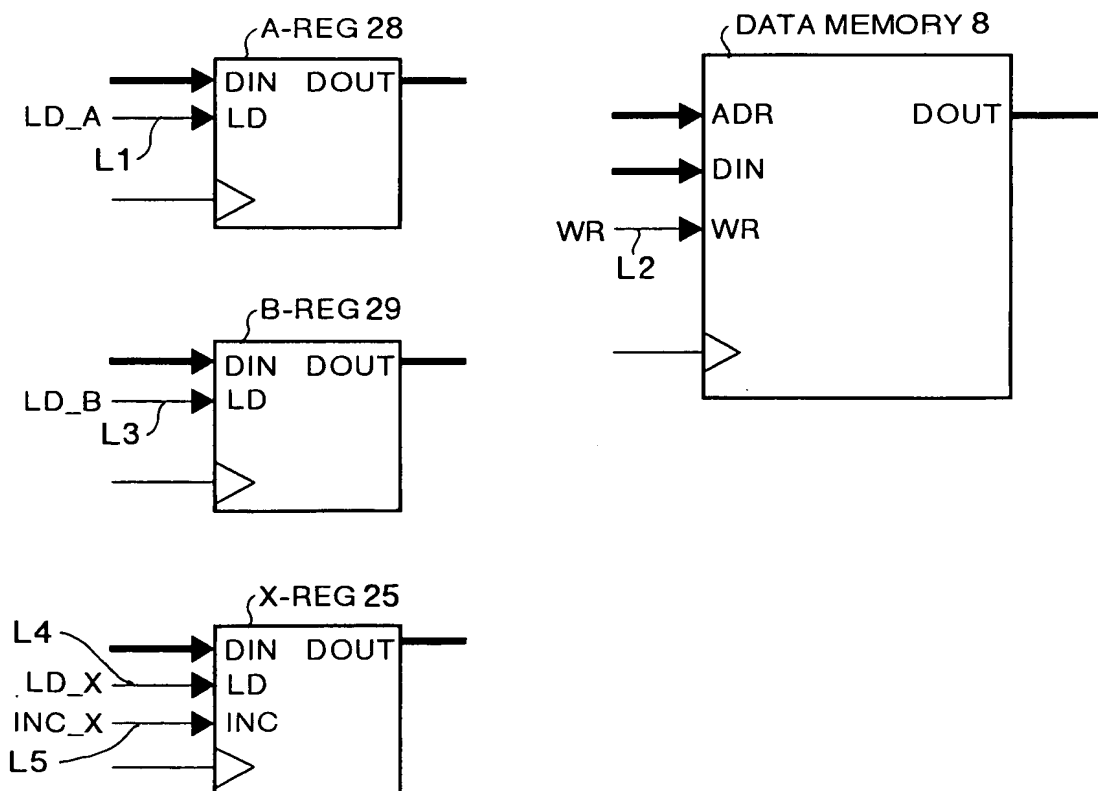


FIG.8



C:CONTROL BIT 1:ENABLE 0:DISABLE



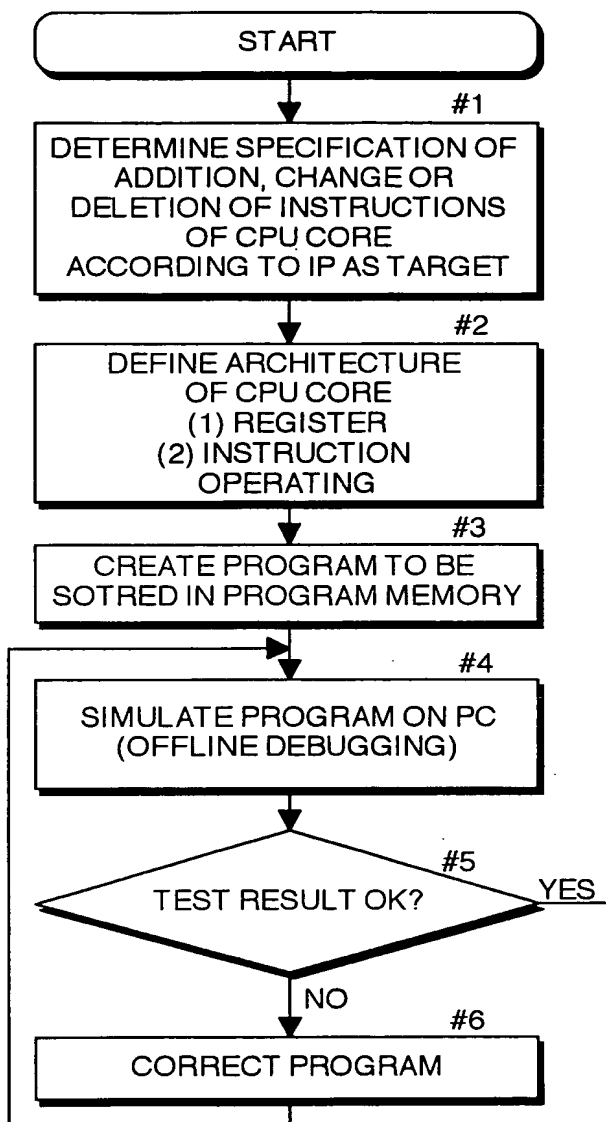


FIG. 10

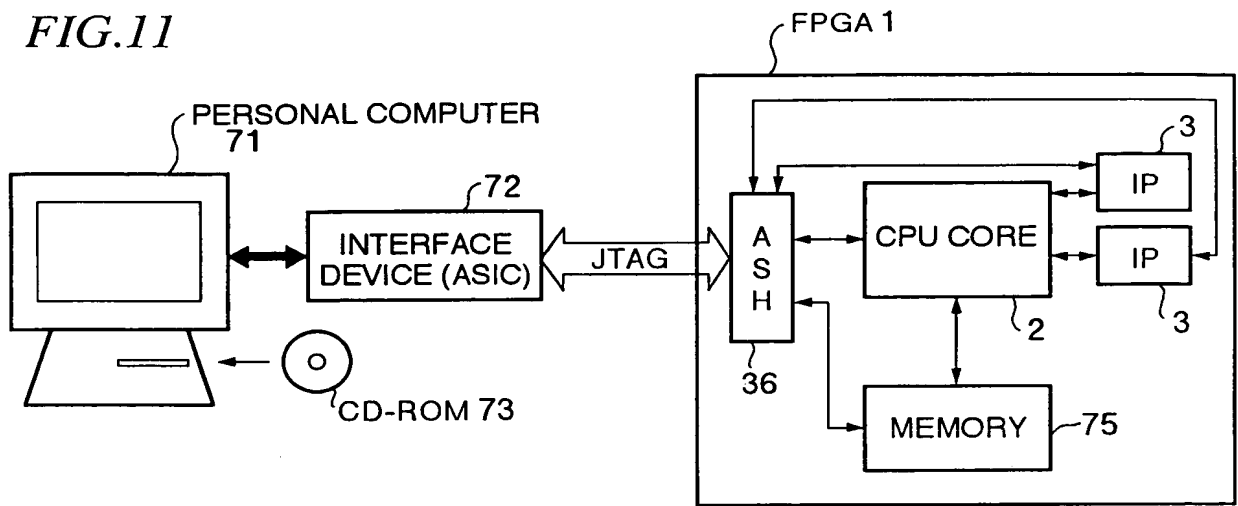


FIG. 12

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CUSTOMIZE CPU CORE

REGISTER (R)

REG. NAME	BIT LENGTH	INITIAL VALUE	REG. TYPE
a	16	h"0000"	GENERAL PURPOSE REG.
b	16	h"0000"	GENERAL PURPOSE REG.
z	1	b"0"	ZERO FLAG
.	.	.	.
.	.	.	.

DEFINE REGISTER

ADD

EDIT

DELETE

SET

CANCEL

HELP

INSTRUCTION (I)

INSTRUCTION NAME	MICRO-CODE	OPERATION DEFINITION
bge	h"9815FFFF"	"if(\$1==0 or \$z==1)\$pc : =op[11:0] : "
emm	h"10A50000"	"\$msk : =op[3 : 0] : "
.	.	.
.	.	.
.	.	.

DEFINE INSTRUCTION OPERATING

ADD

EDIT

DELETE